CLAIMS

What is claimed is:

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A computer system comprising:

a cache memory having a plurality of cache lines each of which stores

3 data;

a storage area to store a data operand; and

an execution unit coupled to said storage area to operate on data elements in said data operand to invalidate data in a predetermined portion of the plurality of cache lines in response to receiving a single instruction.

2. The computer system of Claim 1, wherein the data operand is a register location.

3. The computer system of Claim 2, wherein the register location contains a portion of a starting address of the cache line in which data is to be invalidated.



The computer system of Claim 3, wherein the portion of the starting address includes a plurality of most significant bits of the starting address.

42390.P5965 KGN/rd Express Mail No.: EL105935317US obje

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- 5.) The computer system of Claim 4, wherein execution unit shifts the data elements by a predetermined number of bit positions to obtain the starting address of the cache line in which data is to be invalidated.
- 1 6. The computer system of Claim 1, wherein the predetermined portion 2 of the plurality of cache lines is a page in the cache memory.

A computer system comprising:

a first storage area to store data;

a cache memory having a plurality of cache lines each of which stores

a second storage area to store a data operand; and

an execution unit coupled to said first storage area, said second storage area, and said cache memory, said execution unit to operate on data elements in said data operand to copy data from a predetermined portion of the plurality of cache

- lines in the cache memory to the first storage area, in response to receiving a single
- 10 instruction.

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data;

1 8. The computer system of Claim 7, wherein the data operand is a register

-17-

2 location.

42390.P5965

Express Mail No.: EL105935317US

Patent Application July 20, 1998

1	9.	The computer system of Claim 8, wherein the register location contains
2	a plurality of	of most significant bits of a starting address of the cache line in which
3	data is to be	copied.
M.	10_	The computer system of Claim 9, wherein execution unit shifts the
2	data eleme	nts by a predetermined number of bit positions to obtain the starting
3	address of	the cache line in which data is to be copied.
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::3 :[]		
[=4 [] [
1	11.	The computer system of Claim 7, wherein the predetermined portion
	of the plura	lity of cache lines is a page in the cache memory.
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	12.	The computer system of Claim 7, wherein the execution unit further
	invalidates	data in the predetermined portion of the plurality of cache lines in
3	response to	receiving the single instruction, upon copying the data to the first
4	storage area	• •
		•
1	10	A
1	13	A processor comprising:
2		a decoder configured to decode instructions, and
3		a circuit coupled to said decoder, said circuit in response to a single
4	decoded ins	struction being configured to:
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Patent Application July 20, 1998

42390.P5965 KGN/rd

Express Mail No.: EL105935317US

5		$\int_{\mathbb{R}}$ obtain a starting address of a predetermined area of a cache
6		memory on which the instruction will be performed;
7		invalidate data in the predetermined area of cache memory.
1	14.	The processor of Claim 13, wherein a portion of the starting address is
2		register specified in the decoded instruction.
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1	15.	The processor of Claim 13, wherein the portion of the starting address
2 ;	includes a p	lurality of most significant bits of the starting address.
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Ē	0 16.	The processor of Claim 15, wherein the circuit shifts the data elements
2	by a predet	ermined number of bit positions to obtain the starting address of the
than that it is a standard than it	cache line ii	n which data is to be invalidated.
1	17.	The processor of Claim 13, wherein the predetermined portion of the
2	plurality of o	cache lines is a page in the cache themory.
l	18.	A processor comprising:
2		a decoder configured to decode instructions, and
3		a circuit coupled to said decoder, said circuit in response to a single
Į	decoded inst	ruction being configured to:
	42390.P5965	-19- Patent Applicatio

KGN/rd Express Mail No.: EL105935317US

July 20, 1998

5		Optain a starting a	iddress of a	predetermin	ed area of a cache
6		memory on which the is	nstruction v	will be perfor	med;
7		copy data in the p	oredetermin	ed area of ca	che memory;
8		store the opied data in a	a storage ar	ea separate f	rom the cache memory.
1	19.	The processor of Claim 1	18, wherein	a portion of	the starting address is
2	located in a	register specified in the d	lecoded inst	ruction.	
45	20.	The processor of Claim 1	18, wherein	the portion of	of the starting address
	includes a p	plurality of most significan	t bits of the	starting add	ress.
Ī	O 21.	The processor of Claim 2	20, wherein	the circuit sl	nifts the data elements
2		termined number of bit po	sitions to o	btain the star	ting address of the
	cache line i	n which data is to be copie	ed.		
1	22.	The processor of Claim	0, wherein	the predeter	mined portion of the
2	plurality of	cache lines is a page in the	e cache mer	nory.	
1	23.	The processor of Claim 2	20, wherein	said circuit	further invalidates the
2	data in the J	predetermined portion of	the pluxalit	y of cache lir	es in response to
3	receiving th	e single instruction, upon	copying the	e data to the	storage area.
	42390 P5065		-20-	\	Patent Application

KGN/rd Express Mail No.: EL105935317US Patent Application July 20, 1998

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1	24. A	A computer-implemented method, comprising:
2	a	a) decoding a single instruction;
3	b	in response to said step of decoding the single instruction,
4	obtaining a sta	arting address of a predetermined area of a cache memory on which
5	the single inst	ruction will be performed; and
6	c	completing execution of said single instruction by invalidating
7	data in the pre	edetermined area of cache memory.
u	•	
Ĺ	25. T	The method of Claim $2\frac{1}{4}$, wherein c) comprises setting an invalid bit
that It It them the Same products that	corresponding	to the predetermined area of cache memory.
į	26. T	The method of Claim 24, wherein b) comprises:
	<i>O</i> b	o.1) obtaining a portion of the starting address from a storage
3	location specif	fied in the decoded instruction
<i>4</i>	b	2.2) shifting the portion of the starting address by a predetermined
5	number of bit	positions to obtain the starting address of the cache line in which data
6	is to be invalid	lated.
l	27. T	The method of Claim 26, wherein in b. 1) the portion of the starting
2	address contain	ns a plurality of most significant bits of the starting address, and
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-21-

42390.P5965 KGN/rd Express Mail No.: EL105935317US

3	wherein in b.2), the predetermined number of bit positions represent the number of
4	least significant bits of the starting address.
1	28. The method of Claim 24, wherein the predetermined portion of the
2	plurality of cache lines is a page in the cache memory.
1	29. A computer-implemented method, comprising:
2	a) decoding a single instruction;
3	b) in response to said tep of decoding the single instruction,
5: 14: 15: 16: 17.	obtaining a starting address of a predetermined area of a cache memory on which
5	the single instruction will be performed; and
6	c) completing execution of said single instruction by copying data
7	in the predetermined area of cache memory and storing the copied data in a storage
15 1	30. The method of Claim 29, wherein c) comprises setting an invalid bit
2	corresponding to the predetermined area of cache memory.
1	31. The method of Claim 29, wherein b) comprises:
2	b.1) obtaining a portion of the starting address from a storage
3	location specified in the decoded instruction;

-22-

42390.P5965

KGN/rd Express Mail No.: EL105935317US

4	b.2) shifting the portion of the starting address by a predetermined
5	number of bit positions to obtain the starting address of the cache line in which data
6	is to be invalidated.
1	32. The method of Claim 31, wherein in b.1) the portion of the starting
2	address contains a plurality of most significant bits of the starting address, and
3	wherein in b.2), the predetermined number of bit positions represent the number of
4	least significant bits of the starting address.
	33. The method of Claim 29, wherein the predetermined portion of the plurality of cache lines is a page in the cache memory. 34. The method of Claim 29, further comprising: d) invalidating the data in the predetermined portion of the plurality of cache lines in response to receiving the single instruction, upon copying the data to the storage area.
1	35. A computer-readable apparatus, comprising:
2	a computer-readable medium that stores an instruction which when executed
3	by a processor causes said processor to:
4	obtain a starting address of a predetermined area of a cache memory on
5	which the instruction will be performed; and
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42390.P5965 KGN/rd Express Mail No.: EL105935317US

9

invalidate data in the predetermined area of cache memory. 6 1 36. A computer-readable apparatus comprising: a computer-readable medium that stores an instruction which when executed 2 3 by a processor causes said processor to: obtain a starting address of a predetermined area of a cache memory on 4 5 which the instruction will be performed; copy data from the predetermined area of cache memory; and 6 7 store the copied data in a storage area separate from the cache memory. ij The apparatus of Claim 36, wherein the instruction further causes the 37.

processor to:

invalidate the data in the predetermined portion of the plurality of cache lines in response to receiving the instruction, upon copying the data to the storage area.

42390.P5965

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